PTO/SB/21 (08-00)

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TRANSMITTAL FORM (to be used for all correspondence after initial filing)				Applica	tion Number	imber 09/802,017		-1
				Filing Date		March 8, 2001		
				First N	amed Inventor	Ashley Saul	sbury	_
				Group /	Art Unit			_
				Examin	er Name			_
otal Number of Pages i	in This	Submission		Attorne	y Docket Number	16747-0099	910US	<u></u>
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Fee Transmittal Fo	rm		Assignment Papers (for an Application)		Group	wance Communication to		
Fee Attached			Drawing(s)		Appeals	communication to Board of and Interferences		
Amendment / Resp	onse		Licensing-related Papers		Appeal C	Communication to Group lotice, Brief, Reply Brief)		
After Final			Petition Routing Slip (PTO/SB/69) and Accompanying Petition		Proprieta	ary Information		
Affidavits/decla	aration	(s)	Petition to Convert to a Provisional Application		Status Lo	etter		
Extension of Time Request			Power of Attorney, Revocation Change of Correspondence Address		(please io	nclosure(s) dentify below):		
Express Abandonment Request			Terminal Disclaimer Request for Refund			ies of five (5) cited rences		
Third Information Disclosure Statement Under 37 CFR §1.97 and §1.98			☐ CD, N	lumber of				
Certified Copy of Priority Document(s)			Remarks The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430. JAN 1 5 2002 ATURE OF APPLICANT, ATTORNEY, OR AGENT Townsend and Crew LLP and, Reg. No. 40,647					
Response to Missing Parts/ Incomplete Application							CEL	15
Response to Missing Parts under 37 CFR 1.52 or 1.53							Technology 15 20	<u>7</u> 02
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Firm Townsend and Crew LLP Chad S. Hilyard, Reg. No. 40,647						210 		
Signature	(1/12)							
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Signature		July 1 - 1 - 1-	<u></u>	<u>لن برس</u> ر				

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DE 7057100 v1

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TOWNSEND and TOWNSEND and CREW LLP

By: _____

JAN 1 5 2002 Technology Center 2100

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Ashley Saulsbury, et al.

Application No.: 09/802,017

Filed: March 8, 2001

For: VLIW Computer Processing Architecture with On-chip DRAM Usable as Physical Memory or Cache Memory Examiner: Unassigned

Art Unit: 2183

THIRD INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 and §1.98

Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

The references cited on attached form PTO/SB/08A and PTO/SB/08B are being called to the attention of the Examiner. Copies of the references are enclosed. Also enclosed is a copy of the Search/Examination report corresponding to the PCT application. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no

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Substitute for form 1449B/PTO

Sheet

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Application Number 09/802.017 **Filing Date** March 8, 2001 First Named Inventor Saulsbury, Ashley **Group Art Unit**

(use as many sheets as necessary)

Examiner Name 016747-009910US Attorney Docket Number

				U.S. PATENT DOCUI	MENTS	منموز
		U.S. Pa	itent Document			Pages, Columns, Lines,
Examiner Initials	Cite No.	Number	Kind Code ² (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DP-YYYY	Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS							
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Examiner Initials*	Cite No. ¹	Office ³	Number ⁴	Kind Code ⁵ (if known)	Name of Patente Date of Publication of Where Relevant or Application of Cited Document Cited Document MM-DD-YYYY Figures Appear	nt T°	
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	OTHER PRIOR ART NON-PATENT LITERATURE DOCUMENTS						
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	Α	NUMOMURA Y ET AL: "M32R/D-INTEGRATING DRA:. AND MICROPROCESSOR" IEEE MICRO, IEEE INC. NEW YORK, US, vol. 17 no. 6, 1 November, 1997 (1997-11-01), pages 40-48, XP000726003; ISSN: 0272-1732.					
	А	KOZYRAKIS C E ET AL: "SCALABLE PROCESSORS IN THE BILLION-TRANSISTOR ERA: IRAM" COMPUTER, IEEE COMPUTER SOCIETY, LONG BEACH., CA, US, US vol. 20, no. 0 1 September 1997 (1997-09-01), pages 75-78, XP000730003; JSSN: 0018-9162.					
	С	HERRMANN KLAOS, HILGENSTOCK JOERG, PIRSCH PETER: "ARCHITECTURE OF A MULTIPROCESSOR SYSTEM WITH EMBEDDED DRAM FOR LARGE AREA INTEGRATION" 8 October 1997 (1997-10-08), IEEE INTERNATIONAL CONFERENCE ON INNOVATIVE SYSTEMS IN SILICON, PISCATAWAY, NJ, USA; XP002179990					

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Examiner	•	Date	
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